

# On the effect of SOI substrate in silicon nitride resistance switching MIS structures

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Several resistive memory technologies (RRAMs) are prominent, but few are fulfilling the requirements for CMOS integration and meet the commercialization standards. SiN<sub>x</sub> was found to exhibit competitive resistance switching (RS) properties and attractive SiN-based RRAM devices have been recently demonstrated [1-3]. In the majority of the publications, the RS SiN<sub>x</sub> structures are metal-insulator-semiconductor (MIS), meaning that the bottom electrode was n<sup>++</sup> Si. In this work, the fabrication and electrical characterization of a fully compatible CMOS process on SOI substrate of 1R silicon SiN-based resistance switching MIS devices is presented. The RS characteristics are compared with the same devices previously fabricated on bulk silicon. The scope of this work is to benchmark the use of thin SOI film as bottom electrode compared to bulk Si substrates in single MIS RS cells (1R) utilizing low-frequency noise, DC and AC measurements.

Typical round sweep I-V curves are presented in Fig. 1, where the current switching is evident due to the formation (+eV, SET)/ destroy (-eV, RESET) of a conductive filament made of nitrogen vacancies. The series resistance of the bottom electrode was found to be higher on SOI compared to Si wafer, while the SOI substrate devices exhibited self-compliance characteristics as revealed by I-V voltage sweeps and AC impedance measurements. Device-to-device variability of SET and RESET voltages suggest better uniformity for SOI substrates. Low-frequency noise spectral analysis indicated that there is no additional group of characteristic traps related to the SOI substrate.

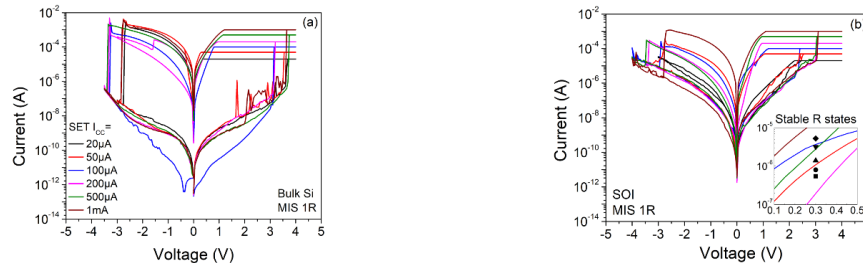


Figure 1: I-V switching characteristics at different I<sub>CC</sub> for a) bulk Si substrate, b) SOI substrate 1R cells. c) SET/RESET voltage statistics.

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## References

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